Sub A1

CLAIMS

1. A memory device comprising:

a plurality of dynamically refreshable memory cells; and

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use;

wherein the memory device is configured to omit refreshing of memory cells that are not in use.

2. A memory device as recited in claim 1, further comprising self-refresh logic on the memory device, wherein the self-refresh logic is configured to not refresh the indicated unused memory cells.

3. A memory device as recited in claim 1, further comprising recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory device is configured to omit refreshing of those memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

4. A system comprising a plurality of memory devices as recited in claim 1, further comprising a memory controller configured to set the use registers to indicate whether the memory cells are unused.

5. A system comprising a plurality of memory devices as recited in claim 1, further comprising a memory controller configured to periodically refresh only those memory cells that are indicated by the use registers to be in use.

6. A system comprising a plurality of memory devices as recited in claim 1, further comprising a memory controller configured to cache at least some of those memory cells that are indicated by the use registers to be in use and to omit refreshing of the cached memory cells.

7. A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a set of memory cells.

8. A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a row of memory cells.

9. A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a bank of memory cells.

10. A memory device as recited in claim 1, wherein the use registers comprise bits that each correspond to a page of memory cells.

11. A memory device comprising:

a plurality of memory cells; and

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are programmable to indicate whether the corresponding groups of memory cells are in use.

12. A memory device as recited in claim 11, further comprising self-refresh logic on the memory device, wherein the self-refresh logic is configured not to refresh unused memory cells.

13. A memory device as recited in claim 11, further comprising recent-access flags associated with respective sets of the memory cells, the recent-access flags being configured to indicate whether the associated sets of memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory device is configured to omit refreshing of those memory cells that are indicated by the recent-access flags to have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval.

14. A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller configured to program the use registers depending on whether the memory cells are being used.

15. A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller that is configured to refresh only those memory cells indicated by the use registers to be in use.

16. A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller that is configured to operate unused memory cells at reduced power.

17. A system comprising a plurality of memory devices as recited in claim 11, further comprising a memory controller configured to cache at least some of those memory cells whose use registers indicate they are not unused and to omit refreshing of the cached memory cells.

18. A memory device as recited in claim 11, wherein the use registers comprise bits that each correspond to a row of memory cells.

19. A system comprising:

one or more memory devices having dynamically refreshable memory cells;

a memory controller configured to periodically refresh the memory cells of the memory devices;

one or more dynamically changeable use registers corresponding respectively to groups of one or more memory cells, wherein the use registers are configurable to indicate whether the corresponding groups of memory cells are in use; and

refresh logic configured not to refresh memory cells that are not in use.

20. A system as recited in claim 19, further comprising recent-access flags associated with the memory cells, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval.

21. A system as recited in claim 19, wherein the memory controller is configured to cache at least some of those memory cells that are not indicated by the one or more use registers to be unused and to omit refreshing of the cached memory cells.

22. A system as recited in claim 19, wherein the use registers are on the memory controller.

23. A system as recited in claim 19, wherein the use registers are on the memory devices.

24. A system as recited in claim 19, wherein the use registers comprise bits that each correspond to a row of memory cells.

25. A system comprising:

memory;

a memory controller;

an operating system configured to dynamically allocate and de-allocate the memory and to identify allocated and de-allocated memory to the memory controller;

wherein the memory controller is responsive to the operating system to operate non-allocated memory at reduced power.

26. A system as recited in claim 25, wherein the memory is dynamically refreshable memory and the memory controller operates the non-allocated memory at reduced power by omitting refreshing of non-allocated memory.

27. A system as recited in claim 25, further comprising recent-access flags associated with the memory, the recent-access flags being configurable to indicate whether corresponding memory cells were accessed in a manner that refreshed the memory cells during a previous refresh cycle interval, wherein the memory controller is configured not to refresh those memory cells that are indicated to have been accessed in a manner that refreshed the memory cells during the previous refresh cycle interval.

28. A system as recited in claim 25, wherein memory controller is configured to cache at least some of the allocated memory and to omit refreshing of the cached memory.

29. A system as recited in claim 25, further comprising a plurality of use bits corresponding respectively to memory rows, wherein each use bit being configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated.

30. A system as recited in claim 25, further comprising a plurality of use bits on the memory controller corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller is configured to omit refreshing of memory rows that are not currently allocated.

31. A system as recited in claim 25, wherein the memory comprises a plurality of discrete memory devices, the system further comprising a plurality of use bits on the memory devices corresponding respectively to memory rows, wherein each use bit is configurable to indicate whether its corresponding memory row is currently allocated, and wherein the memory controller configured to omit refreshing of memory rows that are not currently allocated.

32. In a system having dynamically refreshable memory rows, a method of memory power management, comprising:

keeping track of which memory rows are in use and therefore need refreshing;

periodically refreshing those memory rows that are in use; and

omitting refreshing of memory rows that are not in use.

33. A method as recited in claim 32, further comprising:

determining which rows have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of memory rows that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

34. A method as recited in claim 32, further comprising:

caching at least some of the memory rows that are in use; and

omitting refreshing of the cached memory rows.

35. A method as recited in claim 32, wherein keeping track comprises maintaining a plurality of flags corresponding respectively to the memory rows.

36. A memory controller configured to perform actions comprising:

receiving notifications regarding which of a plurality of memory cells are in use; and

operating unused portions of memory in reduced power modes.

37. A memory controller as recited in claim 36, wherein operating unused portions of memory at reduced power modes comprises omitting refreshing of unused memory rows.

38. A memory controller configured to perform actions comprising:

periodically refreshing memory cells;

receiving notifications regarding which memory cells are in use; and

omitting refreshing of those memory cells that are not in use.

39. A memory controller as recited in claim 38, the controller being configured to perform further actions comprising:

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

40. A memory controller as recited in claim 38, the controller being configured to perform further actions comprising:

caching at least some of the memory cells that are in use; and

omitting refreshing of the cached memory cells.

41. An apparatus comprising:

one or more dynamically changeable use registers that are configurable to indicate unused memory cells;

refresh logic that is configured to periodically refresh memory cells that are not indicated to be unused.

42. An apparatus as recited in claim 41, wherein the use registers correspond respectively to sets of memory cells.

43. An apparatus as recited in claim 41, wherein the use registers correspond respectively to rows of memory cells.

44. An apparatus as recited in claim 41, wherein the use registers correspond respectively to banks of memory cells.

45. An apparatus as recited in claim 41, wherein the use registers correspond respectively to pages of memory cells.

46. A method comprising:

identifying areas of memory based on usage;

caching the identified areas of memory;

identifying one or more memory devices containing the identified areas of memory; and

setting said one or more identified memory devices to a reduced power mode.

47. A method as recited in claim 46, wherein:

said caching comprises caching all the memory cells of a particular memory device; and

said setting comprises setting said particular memory device to the reduced power mode.

48. A memory controller configured to perform actions comprising:

periodically refreshing memory;

identifying areas of memory based on usage;

caching the identified areas of memory;

operating the identified areas of memory in a reduced power mode.

49. A memory controller as recited in claim 48, wherein operating the identified areas of memory in a reduced power mode comprises omitting refreshing of the identified areas.

50. A memory controller as recited in claim 48, wherein operating the identified areas of memory in a reduced power mode comprises setting one or more memory devices to a reduced power mode.

51. A memory controller as recited in claim 48, wherein:

said caching comprises caching all the memory cells of a particular memory device; and

said setting comprises setting said particular memory device to the reduced power mode.

52. A method comprising:

periodically refreshing memory cells;

keeping track of which memory cells have been accessed in a manner that refreshed the memory cells during a previous refresh cycle interval; and

omitting refreshing of those memory cells that have been accessed in a manner that refreshed the memory cells during the previous refresh cycle.

53. A memory controller as recited in claim 52, further comprising:

receiving notifications regarding which memory cells are in use; and

omitting refreshing of those memory cells that are not in use.